ABSTRACT OF THE DISCLOSURE

An apparatus and method for generating early status flags in a pipeline microprocessor is disclosed. The apparatus includes early status flag generation logic that receives an instruction, an early result of the instruction, and a valid indicator of the early result and responsively generates the early flags. If the instruction is flag-modifying, then the early status flags are stored in an early flags register. The early flags in the register are invalidated if the early result from which they are generated is invalid. The early status flags and associated valid indicator may be employed by subsequent conditional instructions for early execution to avoid delay in waiting for the architected status flag values to be generated by execution units later in the pipeline. The early flags are revalidated if all flags-modifying instructions in pipeline stages below the early flag generation logic, if any, have already updated the architected status flags.